**v7.54.0.0**

***(Nov 30th, 2022)***

**IDesignSpec™ (IDS)**

**General Enhancements**

1. F#16967 - Support for the custom TOC templates in the word output. More Details
2. F#17131 - Support for special character encoding in the HTMLalt2 output. More Details

**Bug Fixes**

**General**

1. F#21604 - Fixed the content issue in the description cell in word, HTMLalt2 output.
2. F#21821 - Fix for the "ext\_signal=prot" property in sv.
3. F#16248 - Fixed the issue of enum description in IP-XACT 2014 input getting removed upon generating with IDS-batch.
4. F#21409 - Removal of the warning message when “access” elements are used on the “addressBlock” and “register” element at the same time while generating reg model from IP-XACT input testcase.

**RTL**

1. F#17131 - Fixed character encoding errors depending on generation level.
2. F#21577 - Fixed external memory partial write access with ext\_byte\_enb and sv\_interface=struct property used on memory.
3. F#21709 - Fixed missing wire connections in HW write pulse synchronizer as cdc\_clock handshake with rtl\_hw\_enb property is used.
4. F#21706 - Fixed generation of Verilog code without write enable where we=false property is used without rtl\_precedence prope
5. rty.
6. F#21588 - Fixed the issue of uniquifying the macro name for the `include of the unique package files for all external CSRs.
7. F#19720 - Fixed removal of unused parameters in case of memory component via property rm\_unused\_param=true on the top component.
8. F#20321 - Fixed issue for capi output with properties inst\_name\_cpp\_style and cheader\_opt, when used together.
9. F#21756 - Fixed issue for hwset/clear property used without hw writable field.
10. F#21315 - Fixed the SECDED issue having “is\_rsv” property on field.
11. F#20962 - Fixed the issue when “cdc.clock” and “hard\_reset” properties are used on the same field.
12. F#21319 - Fixed the issue related to unregistered fields having “is\_rsv” property on field.
13. F#19656 - Fixed the aggregation logic file for blocks having repeat on it with property “aggregation\_logic=third\_party”.
14. F#21330 - Fixed the issue while using “single\_address\_data\_out” property with unregistered fields having sw access “ro”.
15. F#21164 - Fixed the issue faced when parity property is used along with “is\_rsv” property with the register access sw=ro and hw=wo.

**IDS NextGen™ (IDS-NG)**

**Bug Fixes**

1. F#21627 - Fix for missing struct template data, when switching from register view to spreadsheet view and vice-versa.
2. F#21720 - Fixes for the GUI error occuring when incorrect testcases are edited.

**SoC-Enterprise™ (SoC-E)**

**Enhancements**

1. F#21689 - Support for parameter value as decimal by default if radix is not specified by the user. More Details
2. B#2051 - Support for generating compact Verilog code, by default, through direct port mapping and assign statement style Verilog code using -explicit switch in the soc\_generate API. More Details

**Bug Fixes**

1. F#21683 - Fix for removal of the parameters addr\_width & bus\_width being created by default in a module when there is no bus specified in the module. These parameters will now only be generated in modules which will have a bus instance.
2. F#21694 - Fix for supporting deep hierarchy width assignment, parameterized width for soc\_connect command.
3. F#21682 - Fix for suppressing the parameters which were previously getting added unnecessarily while using soc\_create API.
4. F#21695 - Fix for changing net name as wire\_name was not working with assign code style.
5. F#21575 - Fix for assigning a tie value to an externally connected output port.
6. F#21688 - Fix for unintentional parameter assignment of instantiation part in top wrapper using switch explicit in soc\_generate command.
7. B#2033 - Fix for appropriate error message when reverse port range/slice is connected.
8. B#2046 - Fix for passing parameters to an instance.
9. B#2048 - Fix for showing DRC message when connecting extra bits for tie connection or peer/parent connection.
10. B#2050 - Fix for displaying messages when deleting port or bus using the soc\_delete command.
11. B#2030 - Fix for width specification with non-zero based range in port declaration i.e., input[7:4] p.